IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Biju Chandran et al.	Examiner:	James M. Mitchell
Serial No.:	10/023723	Group Art Unit:	2827
Filed:	December 21, 2001	Docket:	884.B14US1
Title:	SEMICONDUCTOR PACKAGE WITH LOW RESISTANCE PACKAGE-TO-DIE INTERCONNECT SCHEME FOR REDUCED DIE STRESSES		
Assignee:	Intel Corporation	Customer No:	21186

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Supplemental Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants request that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicants with the next official communication.

Pursuant to 37 C.F.R. §1.97(c)(2), Applicants hereby authorize the Commissioner to charge the fee of $180.00, as set forth in 37 C.F.R. §1.17(p), and any additional fees deemed necessary, to Deposit Account No. 19-0743.